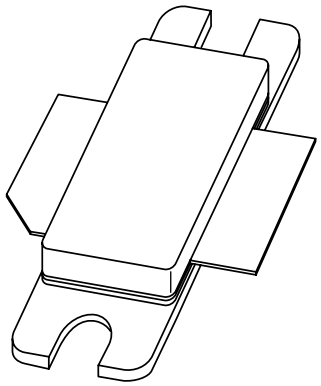
DATA SHEET



BLF1049
UHF power LDMOS transistor

Preliminary specification

2001 Nov 27

Philips
Semiconductors

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UHF power LDMOS transistor BLF1049

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for base station applications (800 MHz to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT502A) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

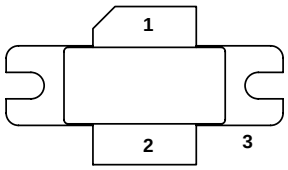


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (dBm)	G_p (dB)	η_D (%)
CW, class-AB	960	28	50	>16	>49

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L avg (W)	G_p (dB)	η_D (%)	ACPR (dB)
EDGE	869	28	45	typ. 17	typ. 25	typ. –65 (1)

Note

1. ACPR 400 kHz at BW = 30 kHz

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
P_{tot}	total power dissipation	T_h = 25 °C	–	700	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to case	T_h = 25 °C; P_{tot} = 700 W; note 1	0.41	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 36 V	–	–	1	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	45	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	–	9	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	–	60	–	mΩ

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 0.41 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (dBm)	G_p (dB)	η_D (%)
CW, class-AB (1-tone)	960	28	550	50	>16	>49

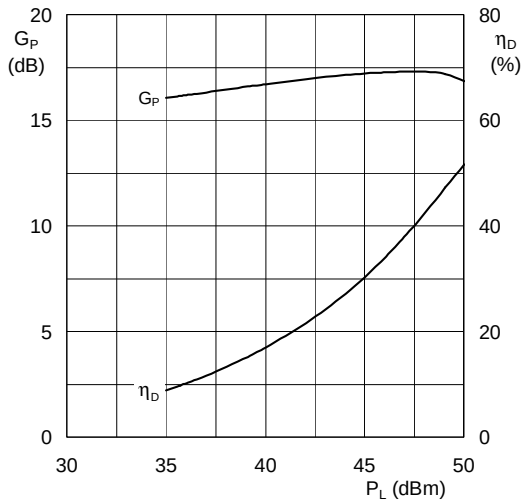
MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L avg (W)	I_{DQ} (mA)	G_p (dB)	η_D (%)	ACPR (dB)
EDGE	869	28	45	800	typ. 17	typ. 25	typ. –65 (1)

Note

1. ACPR 400 kHz at BW = 30 kHz

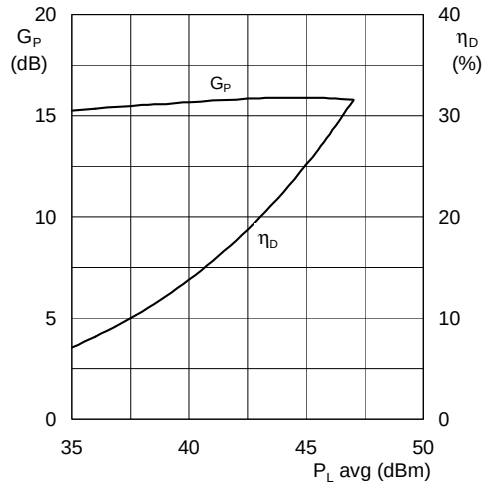
Ruggedness in class-AB operation

The BLF1049 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 960 MHz at rated load power.



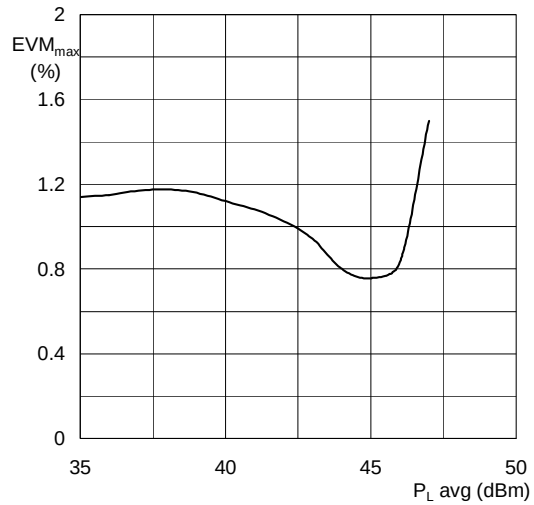
V_{DS} = 28 V; I_{DQ} = 550 mA; P_L = 50 dBm; $T_h \leq 25$ °C

Fig.2 Power gain and drain efficiency as functions of load power; typical values.



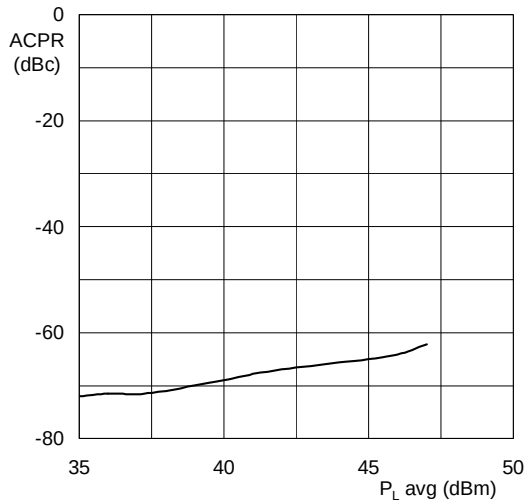
V_{DS} = 28 V; I_{DQ} = 800 mA; f = 869 MHz;
measured under EDGE conditions

Fig.3 Power gain and drain efficiency as functions of load power; typical values.



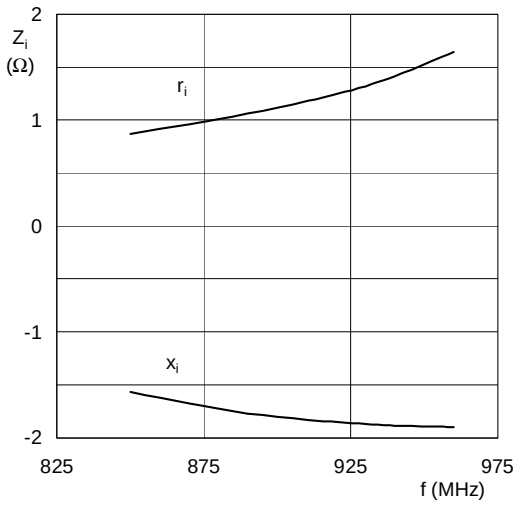
V_{DS} = 28 V; I_{DQ} = 800 mA; f = 869 MHz;
measured under EDGE conditions

Fig.4 Maximum EVM as a function of the average load power, typical values.



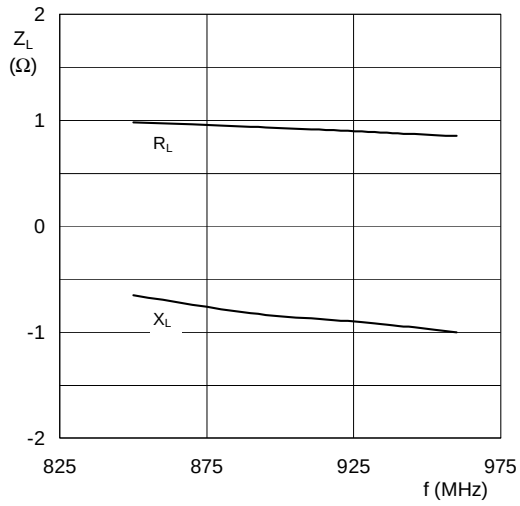
V_{DS} = 28 V; I_{DQ} = 800 mA; f = 869 MHz; Δf = 400 kHz;
measured under EDGE conditions

Fig.5 Intermodulation distortion as a function of the average load power, typical values.



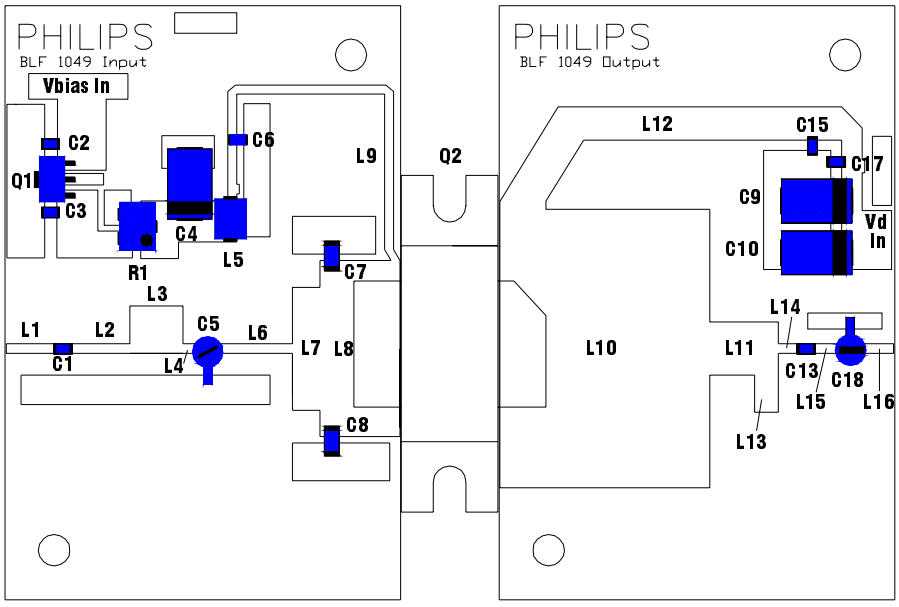
V_{DS} = 28 V; I_{DQ} = 550 mA; P_L = 50 dBm; $T_h \leq 25$ °C

Fig.6 Source impedance as a function of frequency (series components); typical values.



V_{DS} = 28 V; I_{DQ} = 550 mA; P_L = 50 dBm; $T_h \leq 25$ °C

Fig.7 Load impedance as a function of frequency (series components); typical values.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15), thickness 25 mils. The other side is unetched and serves as a ground plane.

Fig.8 Component layout for 800 to 1000 MHz class-AB broadband test circuit.

List of components (see Fig 5)

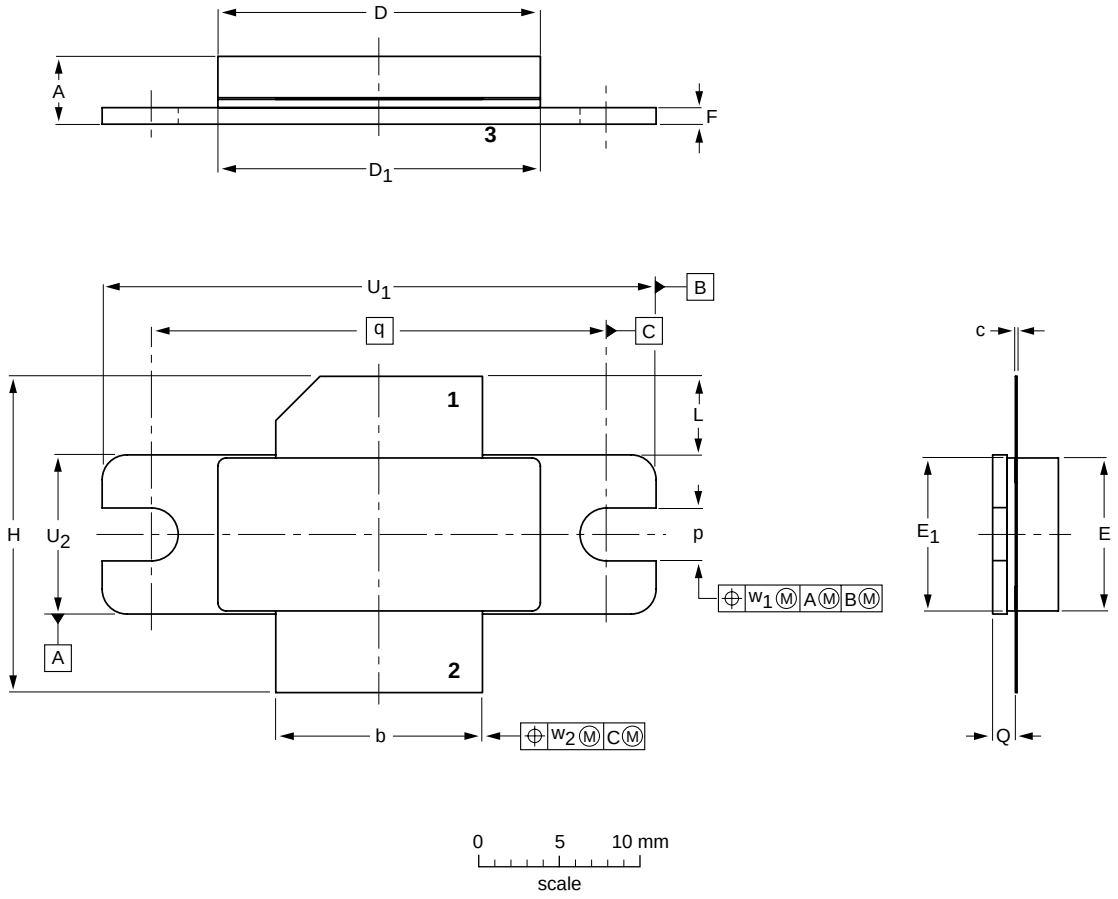
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF		
C2, C3	multilayer ceramic chip capacitor	100 nF		
C4, C9, C10, C11, C12	tantalum capacitor	10 μF		
C5, C18	air trimmer capacitor	4.6 pF		
C7 C8	multilayer ceramic chip capacitor	11 pF		
L1	stripline; note 2		204 × 36 mils	
L2	stripline; note 2		253 × 36 mils	
L3	stripline; note 2		210 × 188 mils	
L4	stripline; note 2		94 × 36 mils	
L5	Ferrox cube			
L6	stripline; note 2		340 × 36 mils	
L7	stripline; note 2		110 × 420 mils	
L8	stripline; note 2		319 × 700 mils	
L9	stripline; note 2		1724 × 36 mils	
L10	stripline; note 2		721 × 1106 mils	
L11	stripline; note 2		389 × 210 mils	
L12	stripline; note 2		1470 × 131 mils	
L13	stripline; note 2		470 × 170 mils	
L14	stripline; note 2		92 × 36 mils	
L15, L16	stripline; note 2		165× 36 mils	
R1	variable resistor	1 kΩ		
Q1	7808 voltage regulator			
Q2	BLF1049 LDMOS transistor			

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (εr = 6.15); thickness 25 mils.

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						~~99-10-13~~ 99-12-28

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For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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